SHARP

NEW PRODUCT INFORMATION

LH5324C00

24M-bit Mask-Programmable ROM

■ Description

The LH5324C00D (User's No. : LH536CXX) is a CMOS 24M-bit mask-programmable ROM organized as 1 572 864× 16 bits. It is fabricated using sillicon-gate CMOS process technology.

■ Features

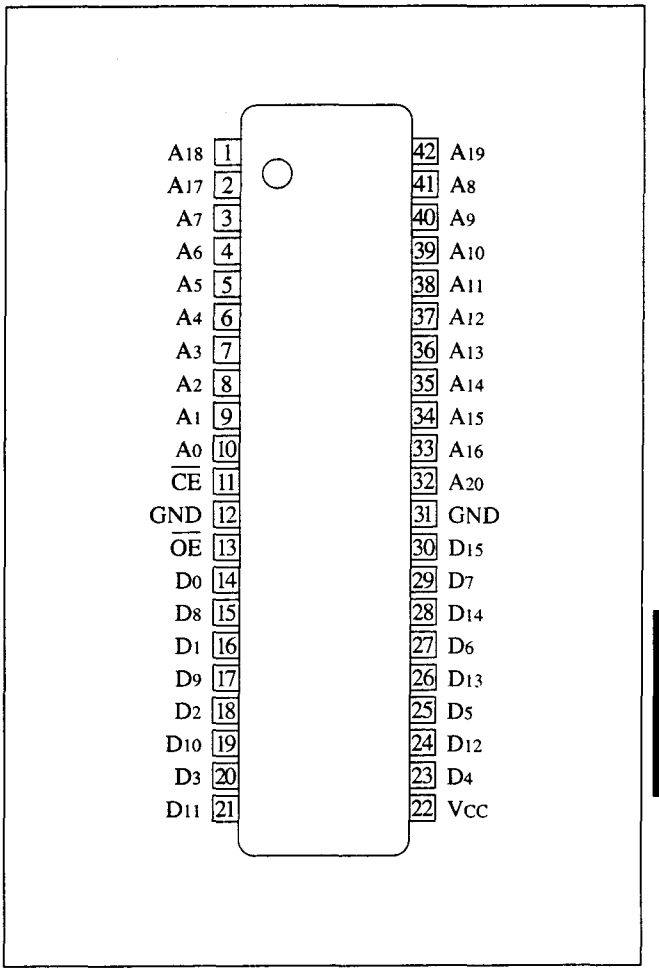
1. 1 572 864×16 bit organization
2. Maximum access time 120 ns
3. Maximum supply current
   - Operating 80 mA
   - Standby 100 μA
4. Static operation (Internal sync. system)
5. TTL compatible I/O
6. Three-state outputs
7. Supply voltage 5 V±10%
8. Package
   - 42-pin DIP (DIP042-P-0600)

■ Pin Description

Signal	Pin name	Note
A_0-A_{20}	Address input	1
D_0-D_{15}	Data output	
$\overline{CE}$	Chip enable input	
$\overline{OE}$	Output enable input	
V_{CC}	Power supply	
GND	Ground	

Note 1. When the address input at both A_{19} and A_{20} is high level, the data outputs become high impedance.
Because this address area does not have data.

■ Pin Connections



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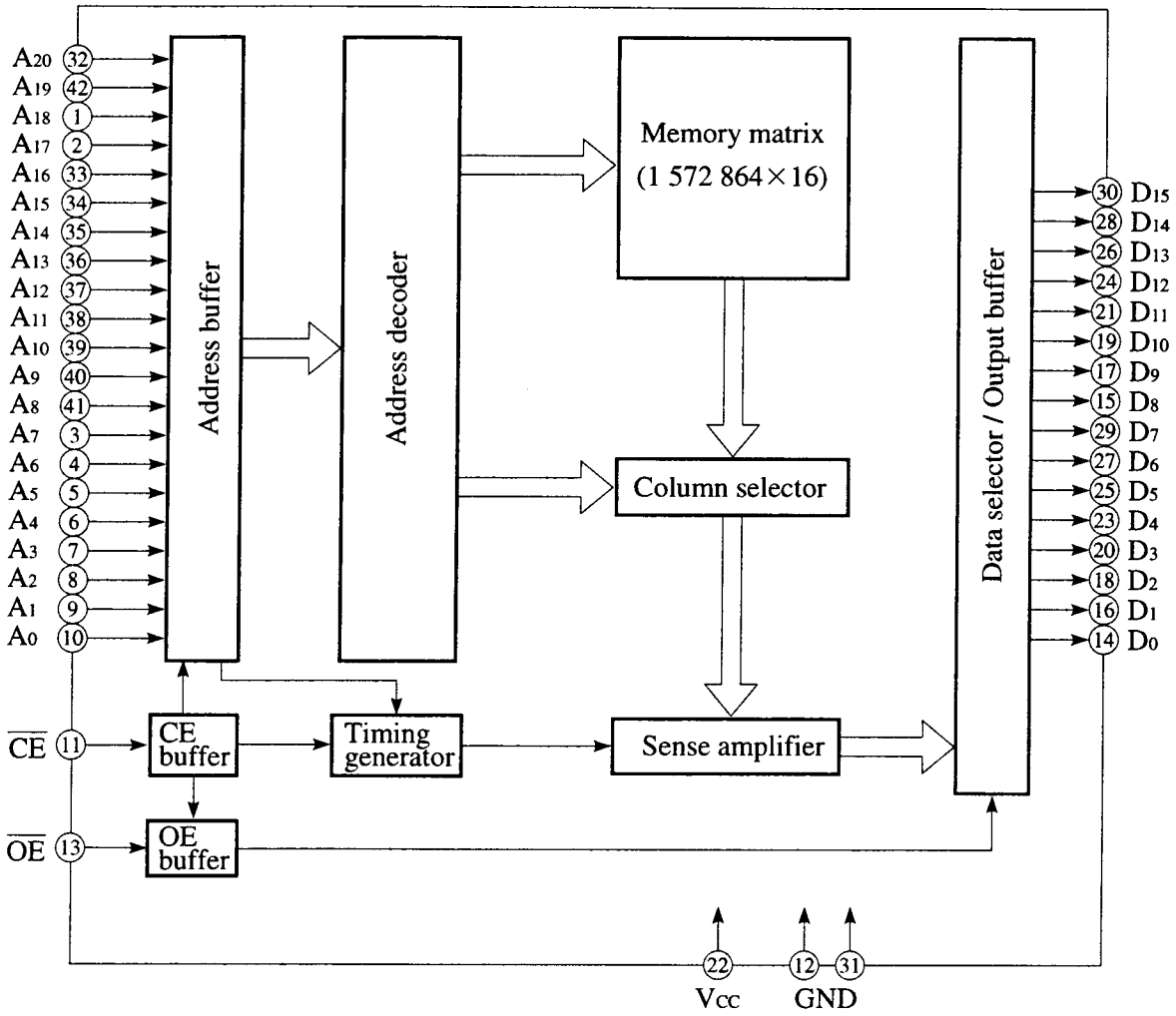
Block Diagram



■ Truth Table

$\overline{CE}$	$\overline{OE}$	A_0-A_{18}	A_{19}	A_{20}	Data output	Supply current
High	X	X	X	X	High impedance	Standby
Low	High	X	X	X	High impedance	Operating
Low	Low	X	Low	Low	Output	Operating
Low	Low	X	Low	High	Output	Operating
Low	Low	X	High	Low	Output	Operating
Low	Low	X	High	High	High impedance	Operating

X : Don't Care

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	−0.3 to +7.0	V
Input voltage	V_{IN}	−0.3 to V_{CC}+0.3	V
Output voltage	V_{OUT}	−0.3 to V_{CC}+0.3	V
Operating temperature	T_{opr}	0 to 70	℃
Storage temperature	T_{stg}	−65 to +150	℃

■ Recommended Operating Conditions

(Ta=0 to 70 ℃)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V

■ DC Characteristics

(V_{CC}=5 V±10%、Ta=0 to 70 ℃)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	Note
Input "High" voltage	V_{IH}		2.2		V_{CC}+0.3	V	
Input "Low" voltage	V_{IL}		−0.3		0.8	V	
Output "High" voltage	V_{OH}	I_{OH}=−400 μA	2.4			V	
Output "Low" voltage	V_{OL}	I_{OL}=2.0 mA			0.4	V	
Input leakage current	$\lvert I_{LI} \rvert$	V_{IN}=0 V, V_{CC}			10	μA	
Output leakage current	$\lvert I_{LO} \rvert$	V_{OUT}=0 V, V_{CC}			10	μA	2
Supply current (Operating)	I_{CC1}	t_{RC}=120 ns			80	mA	
	I_{CC2}	t_{RC}=1.0 μs			70	mA	3
Supply current (Standby)	I_{SB1}	$\overline{CE}$=V_{IH}			2.0	mA	
	I_{SB2}	$\overline{CE}$=V_{CC}−0.2 V			100	μA	
Input capacitance	C_{IN}	f=1.0 MHz, Ta=25 ℃			10	pF	
Output capacitance	C_{OUT}				10	pF	

Note 2. $\overline{CE}$=V_{IH}, $\overline{OE}$=V_{IH}

Note 3. V_{IN}=V_{IH}/V_{IL}, $\overline{CE}$=V_{IL} (Output is open)

■ AC Characteristics

(V_{CC}=5 V±10%、Ta=0 to 70 ℃)

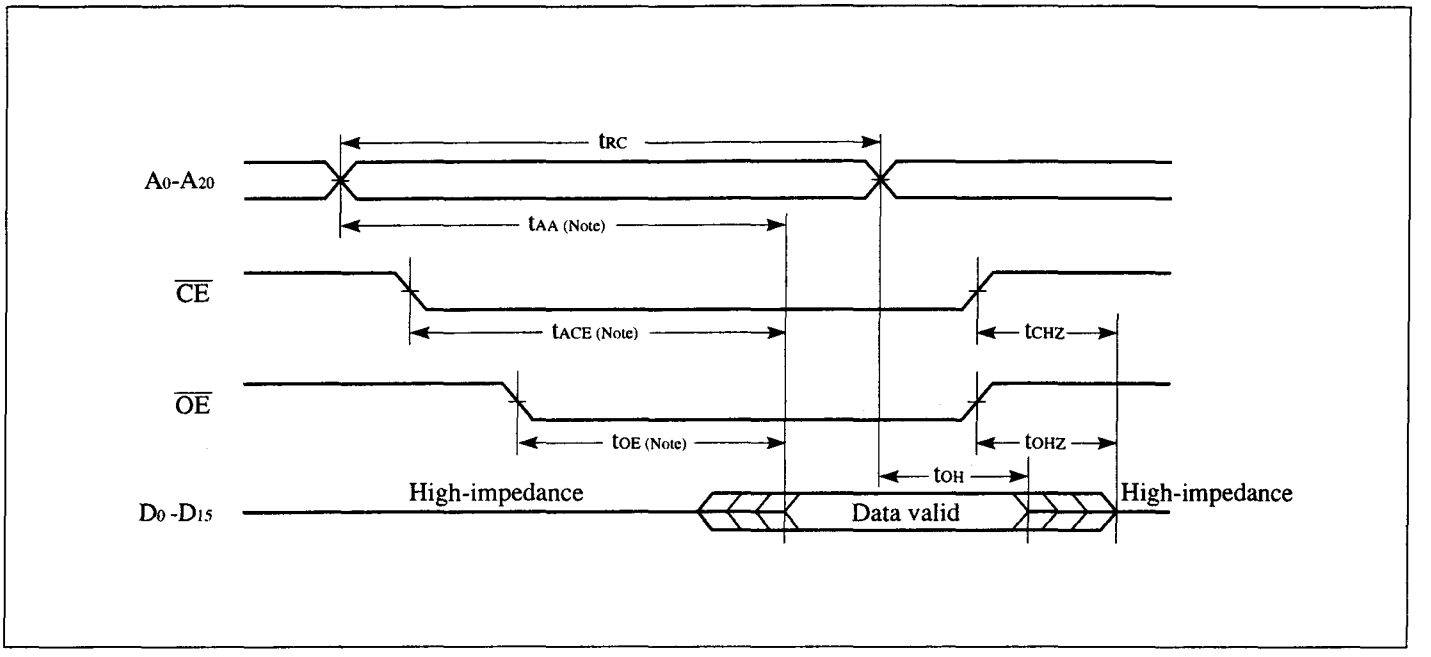
Parameter	Symbol	MIN.	TYP.	MAX.	Unit	Note
Read cycle time	t_{RC}	120			ns	
Address access time	t_{AA}			120		
Chip enable access time	t_{ACE}			120		
Output enable delay time	t_{OE}			60		
Output hold time	t_{OH}	0				
Output floting time	t_{CHZ}			50		4
	t_{OHZ}			50		
	t_{AHZ}			60		

Note 4. Determined by the time for the output to be opened. (Irrespective of output voltage)

AC Test Conditions

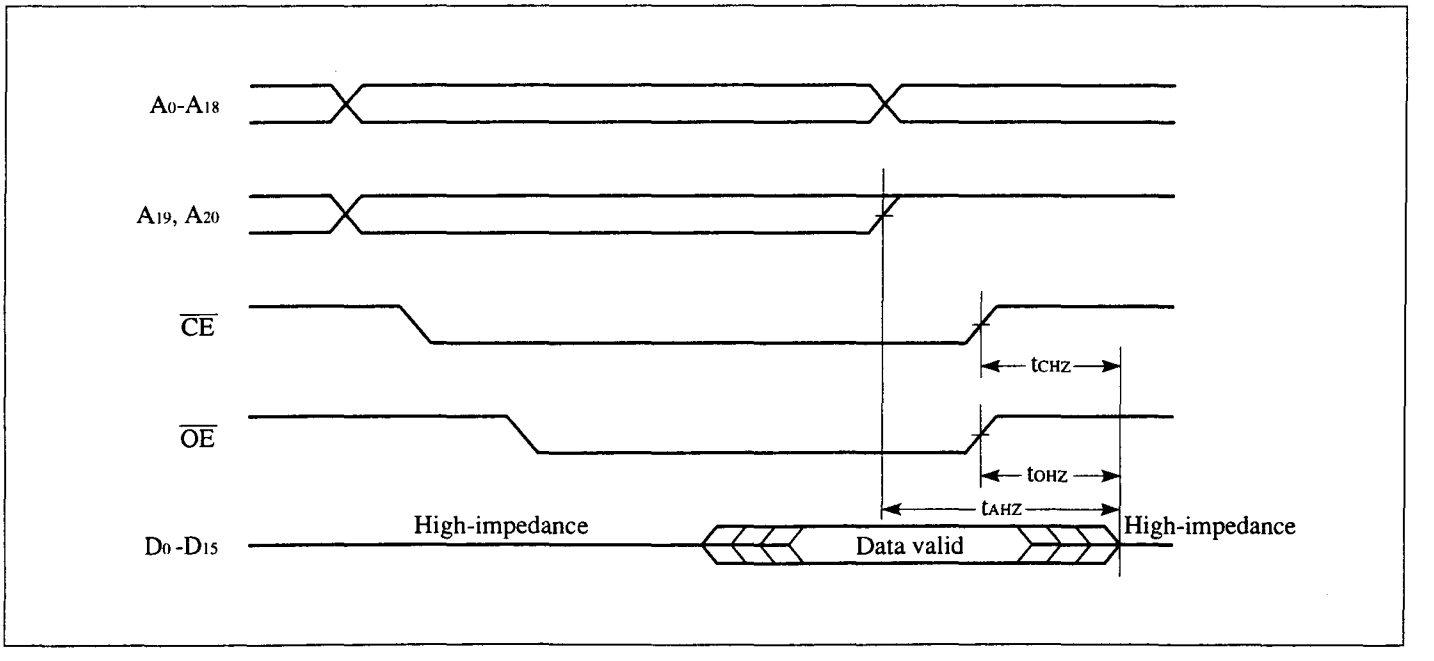
- Input voltage amplitude : 0.6 to 2.4 V
- Input signal rise / fall time : 10 ns
- Input reference level : 1.5 V
- Output reference level : 1.5 V
- Output load condition : 1TTL+100 pF

■ Timing Diagram



Note The output data becomes valid when the last interval t_{AA}, t_{ACE} or t_{OE} have concluded.

〈When the address input at both A_{19} and A_{20} high level〉



■ Sharp's Product Line-up (24M-bit Mask ROM)

★Under development

Configuration (words×bits)	Pinout *	Model No.	User's No.	Access time (ns) MAX. Cycle time (ns) MIN.	Supply current (mA) MAX.	Supply voltage (V)	Package
3M× 8	M	LH5324000D	LH5360XX	150	70	5±10%	42DIP
1.5M×16	M	LH5324C00D	LH536CXX	120	80	5±10%	42DIP
1.5M×16	M	LH5324A00AD	LH536GXX	150	65	5±10%	42DIP
3M× 8 1.5M×16	M	LH5324P00N	LH536PXX	120	80	5±10%	44SOP
3M× 8 1.5M×16	M	★LH5324P00T/TR	LH536DXX	120	80	5±10%	48TSOP (I) forward bend/ 48TSOP (I) reverse bend
3M× 8 1.5M×16	M	LH5324500N	LH5365XX	150	70	5±10%	44SOP

* M : Mask ROM specific pinout